Fabrication of amorphous silicon nanoribbons by atomic force microscope tip induced local oxidation for thin film device applications

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Abstract

We demonstrate the feasibility of induced local oxidation of amorphous silicon by atomic force microscopy. The resulting local oxide is used as mask for the elaboration of thin film silicon resistor. A thin amorphous silicon layer deposited on a glass substrate is locally oxidized following narrow continuous lines. The corresponding oxide line is then used as mask during plasma etching of the amorphous layer leading to the formation of nanoribbon. Such amorphous silicon nanoribbon is used for the fabrication of resistor.

1. Introduction

Owing to their physical and electrical properties silicon nano-objects represent promising elements with strong potential for a large variety of applications. They are currently attracting much attention as components for nanoelectronic devices in integrated silicon technology such as nanowire field effect transistors [1], photonic and optoelectronic devices [2], and chemical or biological sensors [3, 4]. For example, silicon nanowires are useful for the development of innovative electronic devices tanks to their specific properties as high surface to volume ratio, giant piezoresistivity, field emission, and synthesis compatible with large area technology. Silicon nano-objects development could significantly impact areas of electronics, genomics, biomedical diagnosis, drug discovery.... These silicon nano-objects can be prepared by the top-down approach, using various advanced methods such as e-beam [5], deep UV [6] lithography, and more particularly Atomic Force Microscopy (AFM) oxidation of silicon [7]. This latter technique could be used as direct write lithography for fabrication of electronic nano-devices.

Local anodic oxidation (LAO) of silicon surfaces by AFM is a promising method to fabricate nanometer scale oxide patterns due to its very precise control of the feature size. In this technique, a negative voltage is applied to the tip of the AFM system with respect to sample to induce local oxidation. This anodic oxidation (or surface anodisation) is described according to the electrochemical reaction of oxidizing ionic species OH^- from ambient humidity with H-passivated crystalline silicon atoms at the surface of the substrate [8-10].

At first, the native oxide naturally existing on the surface is removed to passivate the silicon surface layer by metastable hydrogenated terminated surface. In this way, the Si-O bonds are substituted by weak Si-H bonds. Then, under a continuous negative bias of the tip, Si-H bonds break and anodisation reaction takes place. The resulting oxide feature depends on experimental conditions (tip bias, write speed, and ambient humidity). For example, previous work reported that electrically conducting AFM tip was used to oxidize regions narrow as 10–30 nm of H-passivated

Si (100) surface at write speeds up to 1 μm/s [11]. In addition, reliability and resolution can be improved by using pulsed voltage instead of continuous polarization [12, 13]. However, in all cases the generated oxide is not as good as thermal oxide, but it can be used as an effective mask for pattern transfer, or as an insulating barrier in the case of very thin metallic or semi conductive film on insulator. With this approach, nanoelectronic devices have already been fabricated [7,14,15].

Most of previous works [7-22] reported tip induced local oxidation process on crystalline silicon substrate and some of them on masking process for fabrication of silicon nano-objects (nanowires or nanodots) by selective liquid anisotropic etching. Thus, owing to these observations, an original way consists to study i) the feasibility of AFM tip induced local oxidation of thin amorphous silicon (a-Si) layer, and ii) the ability of this oxide as mask for fabrication of thin film silicon objects by selective dry etching. Such patterning process compatible with the fabrication of thin silicon film based electronic devices has not been yet demonstrated.

2. Technology and device fabrication

In this study our samples are processed on glass substrate and prepared in clean room under controlled ambient humidity (fixed at 45%). Tip induced local oxidation is performed by using a commercial AFM system (DI-CALIBER) from VEECO instruments company. First, a 250 nm thick SiO_2 buffer layer is deposited by APCVD (Atmospheric Pressure Chemical Vapor Deposition) technique at 390°C on a glass substrate. Then, a 50 nm thick a-Si layer is deposited by LPCVD (Low Pressure CVD) technique at 550°C with a silane (SiH_4) pressure of 90 Pa. The a-Si layer surface is hydrogen passivated into diluted hydrofluoric acid solution (HF-2%). In our case, such hydrogen passivation allows a local oxidation for at least 24 hours. LAO is carried out following continuous narrow lines. Continuous tip bias, V_{tip}, is fixed at -10V and the write speed, s, is 1μm/s. According to these conditions, about 2 nm height with 0.4 μm width oxide long line is

obtained as displayed in the figure 1. The oxide height is typical for local oxide elaborated with similar experimental conditions on crystalline silicon [7,9]. However, as already reported in a previous work [23], local oxidation of a-Si gives wider oxide line than for crystalline silicon. In addition, no significant change of the oxide feature was observed for -10 V < V_{tip} < - 6 V, and for s < 1μm. Such oxide line was then used as mask during a Reactive Ion Etching (RIE) process with SF_6 plasma performed on our samples to etch and thus to pattern a-Si lines. The figure 2 shows the AFM picture of the sample displayed in the figure 1 after plasma etching of the 50 nm thick a-Si layer. The close to 20 nm height resulting a-Si nanoribbon indicates that i) the tip induced local oxide is totally etched by RIE using SF_6 plasma, and consequently that ii) the upper part of the underlying amorphous silicon layer is partially etched. For our process conditions, the SiO_2 versus a-Si etching rate selectivity is difficult to estimate because of the low oxide thickness. Nevertheless, this selectivity is high enough to highlights that tip induced local oxidation by AFM of amorphous silicon can be used as masking process for the fabrication of thin film a-Si objects. However, the width of the resulting nanoribbon is larger (0.8 μm) than the oxide line width (0.4 μm) depicted in the figure 1. This result can be explained by the lateral effect of the field enhanced diffusion of the ionic oxygen species through the growing oxide [8] occurring in the upper part of the amorphous silicon layer. This phenomenon is more pronounced than for crystalline silicon due to the large defect density in the a-Si film. Since an a-Si film has a very large defect density, dangling bonds in the film easily react with oxygen to produce Si-O bonds resulting to a higher growth oxide rate than for crystalline silicon [24]. In addition, another reason involved in the width of the nanoribbon can be the size and the geometry of the tip. These two reasons can explain the formation of a wider buried oxide line that does not appear on the AFM observation (fig. 3 (a)). Consequently this oxide mask induces a wider a-Si pattern after plasma etching (fig. 3 (b)). Improvements in term of aspect ratio (height/width) of the local oxide feature, and therefore of the a-Si nanoribbon feature, could be possible by application of short pulses that restrict the lateral

diffusion of ionic species while a high-voltage pulse produces a fast growth rate in the vertical direction [13].

LAO is therefore used as masking process in order to pattern amorphous silicon for fabrication of thin film silicon resistor. First a 250 nm thick SiO_2 buffer layer is deposited by APCVD technique at 390°C on a glass substrate. Then, a 200 nm thick heavily *in-situ* phosphorus doped amorphous silicon layer is deposited by LPCVD technique at 550°C and 90Pa, and crystallized by a thermal annealing at 600°C under vacuum. The phosphorus concentration of this N^+ type polysilicon (N^+ Poly-Si) layer used as electrode material is 2×10^{20} cm^{-3}. This layer is patterned by classical UV lithography and etched by RIE using SF_6 plasma to define the device electrodes (fig. 4. (a)). Next, a 50 nm thick a-Si layer is deposited and locally oxidized, using conditions previously mentioned, following a continuous line between the two N^+ Poly-Si pads (fig. 4 (b)). An amorphous silicon nanoribbon is then patterned according to the process previously described to interconnect electrodes to achieve electrical resistor (fig. 4 (c)). The 3D AFM pictures of the device represented in figures 5 (a) and (b) show a uniform and continuous 2 μm long × 0.8 μm width × 20 nm thick a-Si nanoribbon. I(V) characteristics of such resistor is measured at room temperature by a 4156 B semiconductor parameter analyzer. Results plotted in figure 5 (c) highlight an ohmic electrical connection at the a-Si nanoribbon/N^+ Poly-Si electrode interfaces. In addition, it clearly shows that LAO process operates continuously between the two differently levelled N^+ Poly-Si pads. The estimated value of the corresponding resistor is 40MΩ.

3. Conclusion

Feasibility of LAO of amorphous silicon film by atomic force microscopy is shown to get a few micrometers long, uniform, and continuous oxide lines. The corresponding tip induced local oxide can be used as etch mask for elaboration of few nanometers thick film silicon patterns by selective dry etching. However, improvements are necessary to reduce the width of line-patterns in

particular for the fabrication of nanowires. This work is the first step towards the fabrication of thin film silicon nanodevices using AFM local oxidation of silicon as direct write lithography system.

References

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Figure captions

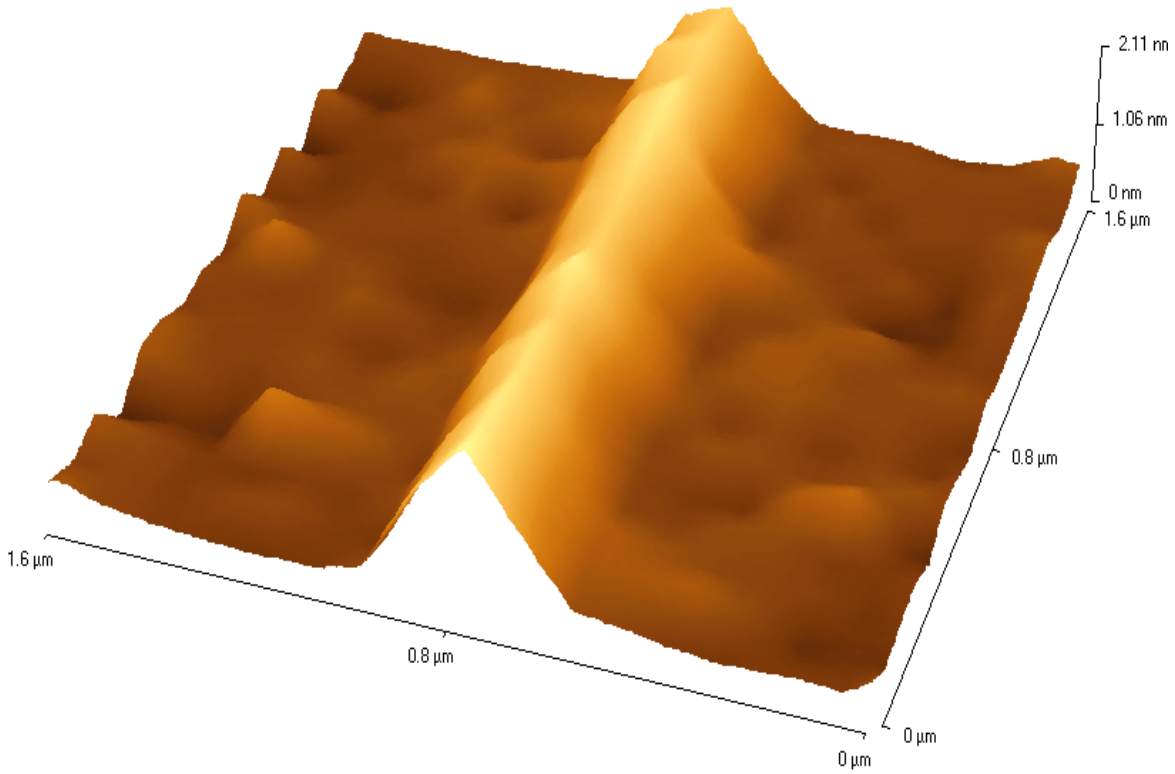
Figure 1: (a) AFM picture of oxide line obtained by AFM local oxidation of a-Si layer. (b) Maximum height of the oxide is 2 nm with an average width estimated at the surface is about 0.4 μm.

Figure 2: (a) AFM picture of a-Si nanoribbon obtained after SF_6 plasma etching of the sample represented in the figure 1. (b) The average nanoribbon height is about 20 nm with an average width estimated about 0.8 μm.

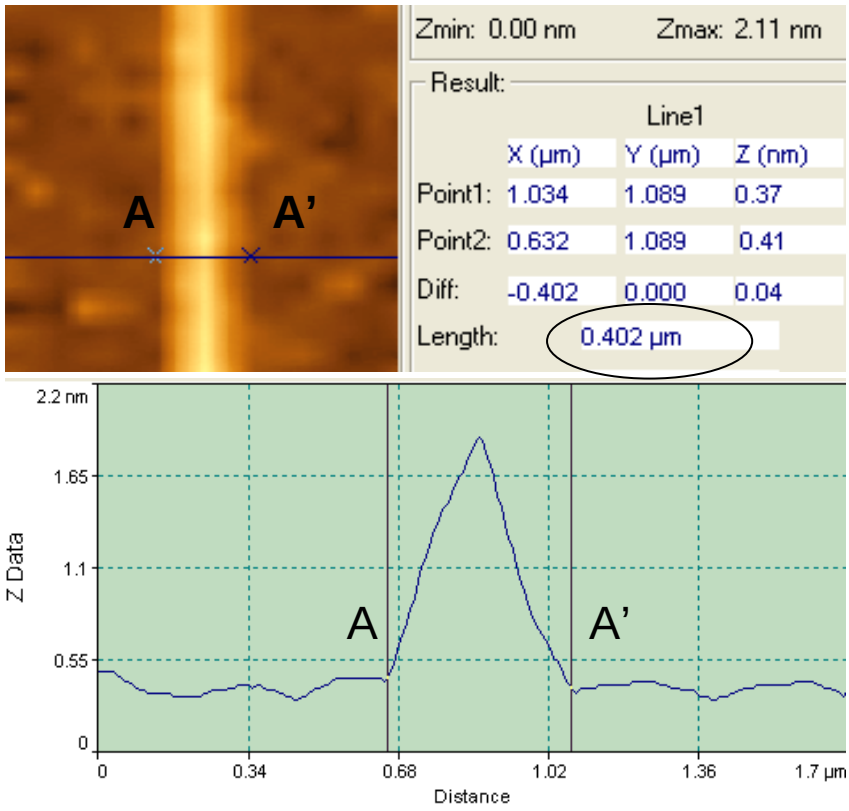
Figure 3: (a) Schematic illustration of a wider buried oxide due to the lateral effect of the field enhanced diffusion of ionic oxygen species through the growing oxide. (b): wider underlying a-Si pattern obtained after plasma etching using such oxide line mask.

Figure 4: Cross section view of the main technological steps of the a-Si nanoribbon resistor fabrication: (a) N^+ poly-Si layer deposited on glass substrate and plasma etched to define electrodes contacts, (b) AFM tip induced local oxidation of a-Si layer, (c) plasma etching of a-Si layer (formation of the a-Si nanoribbon interconnecting the two N^+ poly-Si electrodes).

Figure 5: (a) 3D AFM picture of a 2 μm long × 0,8 μm width × 20 nm thick a-Si nanoribbon resistor obtained by AFM local oxidation, (b) I(V) characteristics of the resistor.

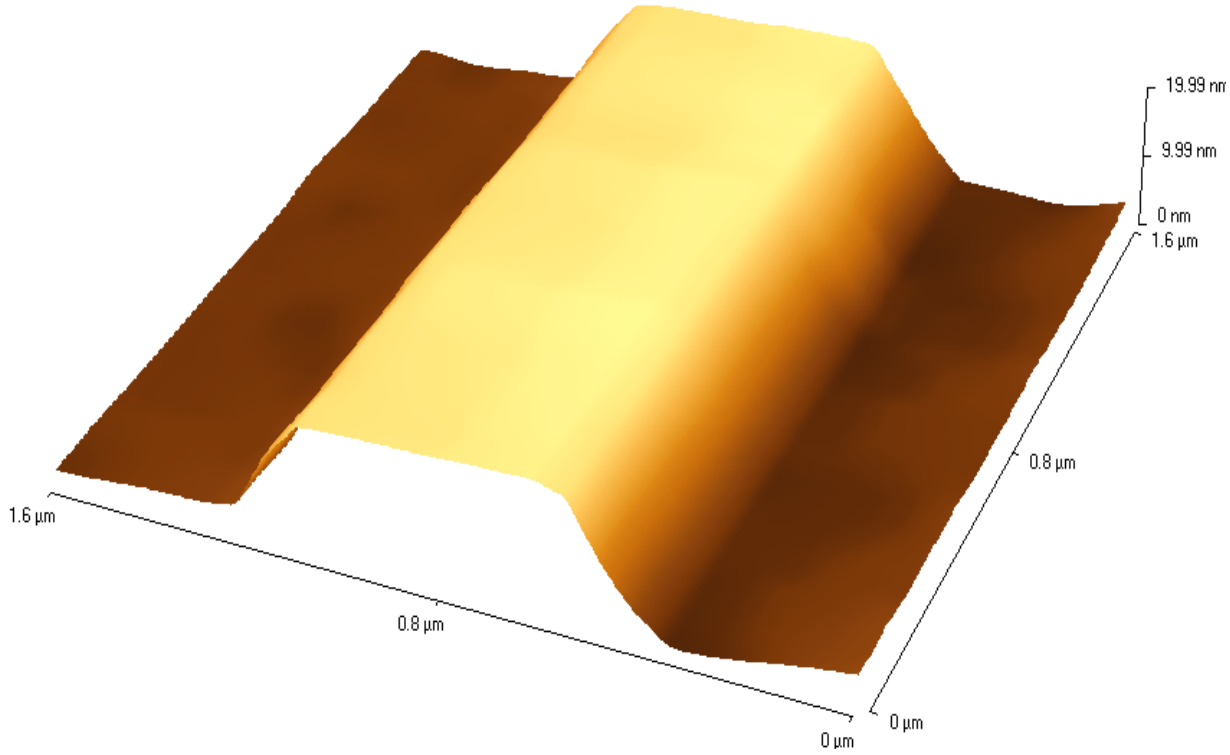

2.11 nm
1.06 nm
0 nm
1.6 µm
0.8 µm
0 µm
1.6 µm
0.8 µm
0 µm

(a)


A
A'
Zmin: 0.00 nm
Zmax: 2.11 nm
Result:
Line1
X (µm)
Y (µm)
Z (nm)
Point1: 1.034 1.089 0.37
Point2: 0.632 1.089 0.41
Diff: -0.402 0.000 0.04
Length: 0.402 µm
2.2 nm
1.65
1.1
0.55
0
Z Data
A
A'
0
0.34
0.68
1.02
1.36
1.7 µm
Distance

(b)

Figure 1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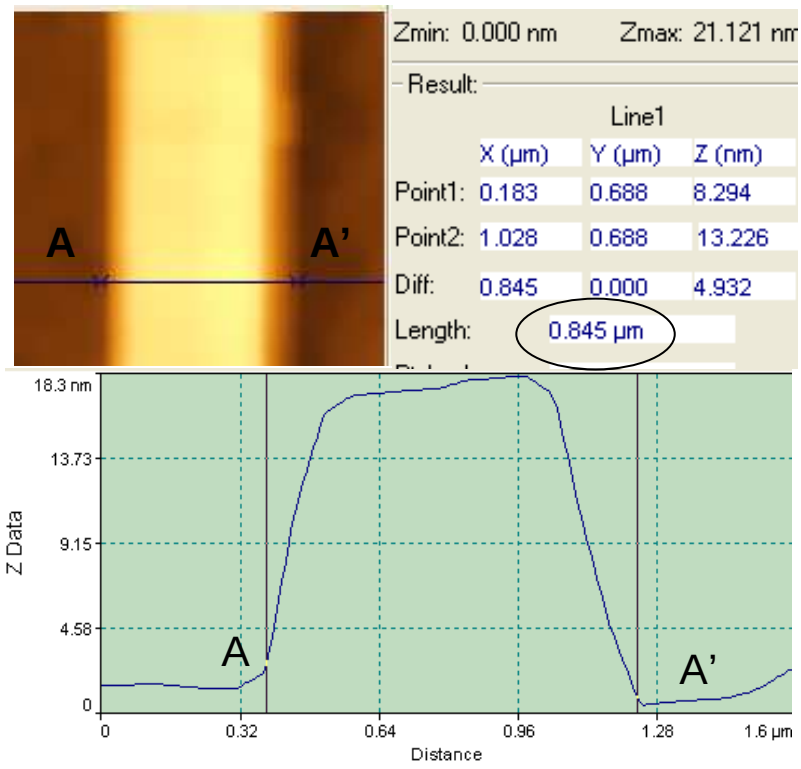
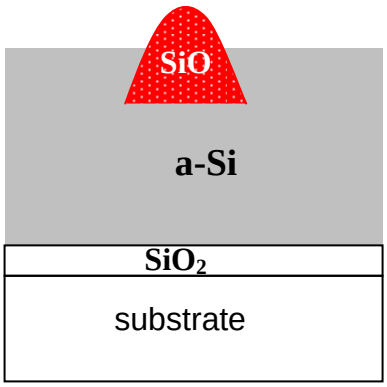
9.99 nm
0 nm
1.6 µm
0.8 µm
0 µm
1.6 µm
0.8 µm
0 µm

(a)

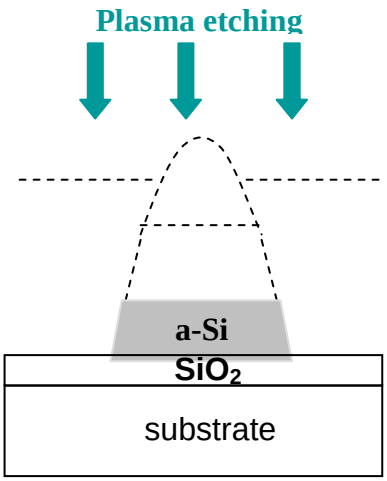

A
A'
Zmin: 0.000 nm
Zmax: 21.121 nm
Result:
Line1
X (µm)
Y (µm)
Z (nm)
Point1: 0.183 0.688 8.294
Point2: 1.028 0.688 13.226
Diff: 0.845 0.000 4.932
Length: 0.845 µm
18.3 nm
13.73
9.15
4.58
0
Z Data
A
A'
0
0.32
0.64
0.96
1.28
1.6 µm
Distance

(b)

Figure 2



(a)



(b)

Figure 3

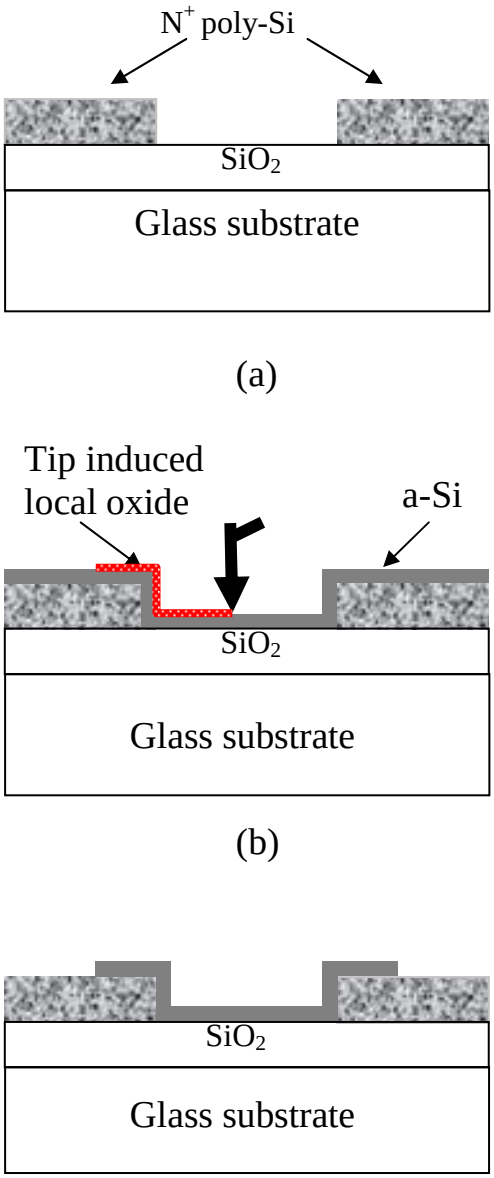
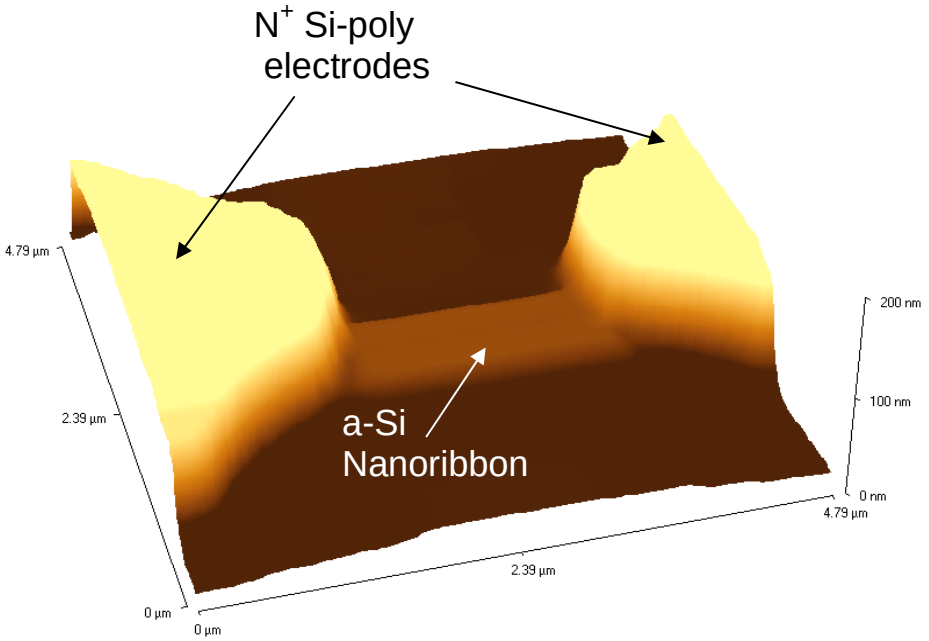
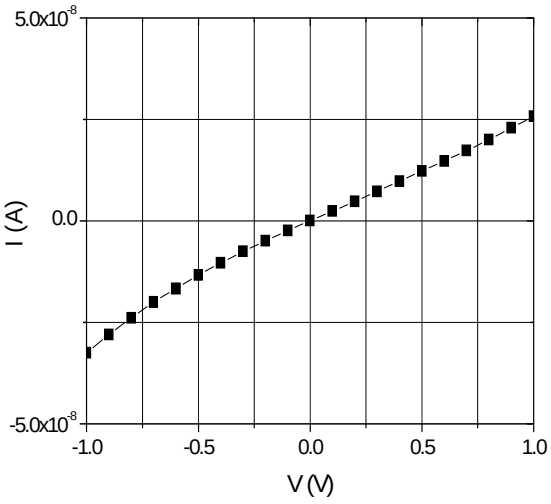

N+ poly-Si
SiO2
Glass substrate
(a)
Tip induced
local oxide
a-Si
SiO2
Glass substrate
(b)
SiO2
Glass substrate

Figure 4


N+ Si-poly
electrodes
a-Si
Nanoribbon
4.79 µm
2.39 µm
0 µm
0 µm
2.39 µm
4.79 µm
200 nm
100 nm
0 nm

(a)


5.0x10-8
0.0
-5.0x10-8
I (A)
-1.0
-0.5
0.0
0.5
1.0
V (V)

(b)

Figure 5